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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,000	10/02/2003	Robert C. Chang	SANDP039	8920

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,000	CHANG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are presented for examination in this application (10,679,000) filed on October 2, 2003.

Acknowledgement is made to the Information Disclosure Statement received on October 27, 2003.

Claim Objections

2. Claim 15 is objected to because of the following informalities: Claim 15 recites "The memory system of claim **1** ..." However, judging from the sequence of the claims, it appears that the intended recitation should be "The memory system of claim **11** ..." Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 6-9, 11-14, 17-20, 22-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carnevale et al. (US 6,353,910), and in view of Payne et al. (US Patent Application Publication 2003/0099140).

As to claim 1, Carnevale et al. disclose **a method for encoding data** [Method and Apparatus for Implementing Error Correction Coding (ECC) in a Dynamic Random Access memory Utilizing Vertical ECC Storage (title)] **associated with a page** [figure 2; a page is considered to be the number of bytes contained in one row of a DRAM

module (column 2, lines 38-57)] **within a non-volatile memory** [taught by Payne et al., see below] **of a memory system** [figure 1 shows the memory system], **the page having a data area and an overhead area** [taught by Payne et al., see below; figure 3 of Carnevale et al. shows the data portion], **the method comprising**:

dividing at least a part of the page into at least two segments of the data [figure 2 shows the pages of data; figure 3 shows that the data is partitioned into a plurality of segments with 4 bytes in each segment], **the at least two segments of the data including a first segment and a second segment** [figure 3 shows that the data is partitioned into a plurality of segments with 4 bytes in each segment];

performing error correction code (ECC) calculations on the first segment to encode the first segment [figure 3 shows that one byte of ECC data is calculated and associated with each of the 4-byte segments; column 2, lines 37-57]; **and**

performing the ECC calculations on the second segment to encode the second segment [figure 3 shows that one byte of ECC data is calculated and associated with each of the 4-byte segments; column 2, lines 37-57], **wherein the second segment is encoded substantially separately from the first segment** [figure 3 shows that one byte of ECC data is calculated and associated with each of the 4-byte segments; column 2, lines 37-57].

With respect to claim 1, the device mentioned in Carnevale et al.'s invention is **DRAM** and **not non-volatile memory devices**, although the scheme disclosed by Carnevale et al. is directly applicable to non-volatile memory devices. Further,

Carnevale et al. do not mention that **the page having a data area and an overhead area**.

However, Payne et al. disclose in their invention "Data Handling system" a method and apparatus for generating ECC data for flash memory [paragraph 0003; note that flash memory is non-volatile] in which the input data comprises information data as well as overhead data [abstract; figures 1 and 2].

The invention of Payne et al. extends the ECC technique to non-volatile memory devices which have both user data area and overhead area, hence improving its flexibility and making it more powerful.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefit of being able to apply ECC technique to both volatile and non-volatile memory devices which have both user data area and overhead area, as demonstrated by Payne et al., and to incorporate it into the existing system disclosed by Carnevale et al. to further improve the flexibility and versatility of the ECC technique.

As to claim 2, Payne et al. teach that **the first segment includes the data area** [the information data (figure 1,12)] **and the second segment includes the overhead area** [header data (figure 1, 14)].

As to claim 3, Carnevale et al. teach that **the first segment includes a first section of the data area** [figure 3 shows that the data is partitioned into a plurality of segments with 4 bytes in each segment; for example, the first segment may consist of byte 0~byte 3] **and the second segment includes a second section of the data**

area [figure 3 shows that the data is partitioned into a plurality of segments with 4 bytes in each segment; for example, the second segment may be any segment in figure 3 other than byte 0~byte 3]

As to claim 6, Carnevale et al. teach **dividing the at least part of the page into the at least two segments of the data includes**:
dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment [figure 3 shows that the data is partitioned into a plurality of segments (more than 3 segments) with 4 bytes in each segment].

As to claim 7, Carnevale et al. teach **performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment** [figure 3 shows that one byte of ECC data is calculated and associated with each of the 4-byte segments; column 2, lines 37-57].

As to claim 8, Carnevale et al. and Payne et al. teach that **the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area** [Carnevale et al. teach that the data is partitioned into a plurality of data segments (more than 3 segments) with 4 bytes in each segment, and Payne et al. teach that one of the segment is the overhead area (header data, figure 1, 14)].

As to claim 9, Carnevale et al. teach that **the first segment includes a first section of the data area, the second segment includes a second section of the**

data area, and the third segment includes a third section of the data area [figure 3 shows that the data is partitioned into a plurality of segments (more than 3 segments) with 4 bytes in each segment].

As to claim 11, refer to "As to claim 1."

As to claim 12, Carnevale et al. teach that **the memory system of claim 11 further including: a controller** [memory controller, figure 1, 104], **the controller being arranged to process the code devices** [figure 4 illustrates logical steps performed by memory controller ... (column 3, lines 20-67)].

As to claim 13, refer to "As to claim 2."

As to claim 14, refer to "As to claim 3."

As to claim 17, refer to "As to claim 6."

As to claim 18, refer to "As to claim 7."

As to claim 19, refer to "As to claim 8."

As to claim 20, refer to "As to claim 9."

As to claim 22, Carnevale et al. teach that **the code devices are one of software code devices and firmware code devices** [figure 4 shows the software procedure for calculating the ECC code for each page].

As to claim 23, refer to "As to claim 1."

As to claim 24, refer to "As to claim 2."

As to claim 25, refer to "As to claim 3."

As to claim 27, refer to "As to claim 6."

As to claim 28, refer to "As to claim 7."

As to claim 29, refer to "As to claim 8."

As to claim 30, refer to "As to claim 9."

5. Claims 4-5, 15-16, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carnevale et al. (US 6,353,910), in view of Payne et al. (US Patent Application Publication 2003/0099140), and further in view of Zhang et al. (US 6,662,333).

As to claim 4, neither Carnevale et al. nor Payne et al. mention that **the ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.**

However, Applicants admit in the Background of the Invention Section of their disclosure that the above recited feature is well known in the art [some ECC algorithms that are used to encode and decode data for storage are known as 1-bit ECC algorithms and 2-bit ECC algorithms ... (paragraph 0009)].

Further, Zhang et al. disclose in their invention "Shared Error Correction for Memory Design" an ECC scheme in which single bit errors are corrected and double bit errors are detected [column 1, lines 24-33].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated by Applicants' admission as well as Zhang et al., hence lacking patentable significance.

As to claim 5, neither Carnevale et al. nor Payne et al. mention that **the ECC Algorithm is a Hamming Code ECC Algorithm**.

However, Zhang et al. teach in their invention "Shared Error Correction for Memory Design" that Hamming Code based ECC algorithms are well known in the art [a well known error correction code is the Hamming code (column 1, lines 55-67)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Zhang et al., hence lacking patentable significance.

As to claim 15, refer to "As to claim 4."

As to claim 16, refer to "As to claim 5."

As to claim 26, refer to "As to claims 4-5."

6. Claims 10, 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carnevale et al. (US 6,353,910), in view of Payne et al. (US Patent Application Publication 2003/0099140), and further in view of Kramer (US 6,182,239).

As to claims 10, 21 and 31, neither Carnevale et al. nor Payne et al. mention that **the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.**

However, the inventions of Carnevale et al. and Payne et al. are directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

7. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Benton et al., (US 5,164,944), "Method and Apparatus for Effecting Multiple Error Correction in a Computer Memory."
- Sinclair et al., (US Patent Application Publication 2003/0156473), "Memory Controller."
- Moro et al., (US 6,769,087), "Data Storage Device and Method for Controlling the Device."
- Purdham, (US 5,666,371), "Method and Apparatus for detecting Errors in a System that Employs Multi-Bit Wide Memory Elements."
- Kellogg et al., (US 5,896,404), "Programmable Burst Length DRAM."

Conclusion

8. Claims 1-31 are rejected as explained above.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 21, 2005

PIERRE BATAILLE
PRIMARY EXAMINER
1/5/06